

## Useful Design 001B:

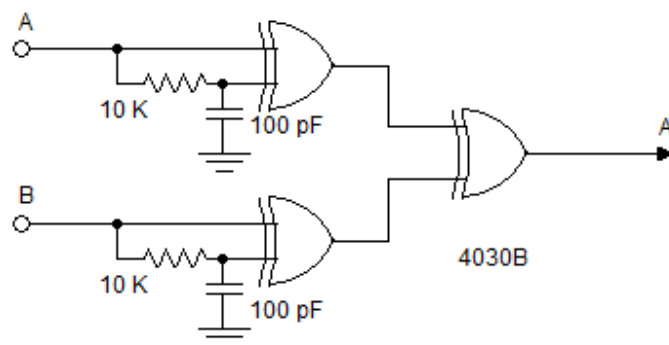
### Improvements for the original “Pulse Encoder to Analog Voltage Circuit” (See Useful Design 001).

**The first improvement is to expand resolution for encoders running slower or with fewer pulses per revolution.**

This is a pulse multiplier made up of CMOS 4030B exclusive or gates. When input “A” transitions from one state to the other, one gate input follows immediately. The other input is delayed by an RC constant which is in this case is one microsecond. This timing difference produces a one microsecond pulse at the gate output, no matter which direction the logic state changes. This makes two pulses for each input pulse on “A”.

Doing the same on the “B” input does the same and because of the phasing of the “A” and “B” inputs, these pulses do not coincide. Adding these pulse strings together in one more exclusive or gate combines the pulse strings in to one string at four times the original “A” input frequency.

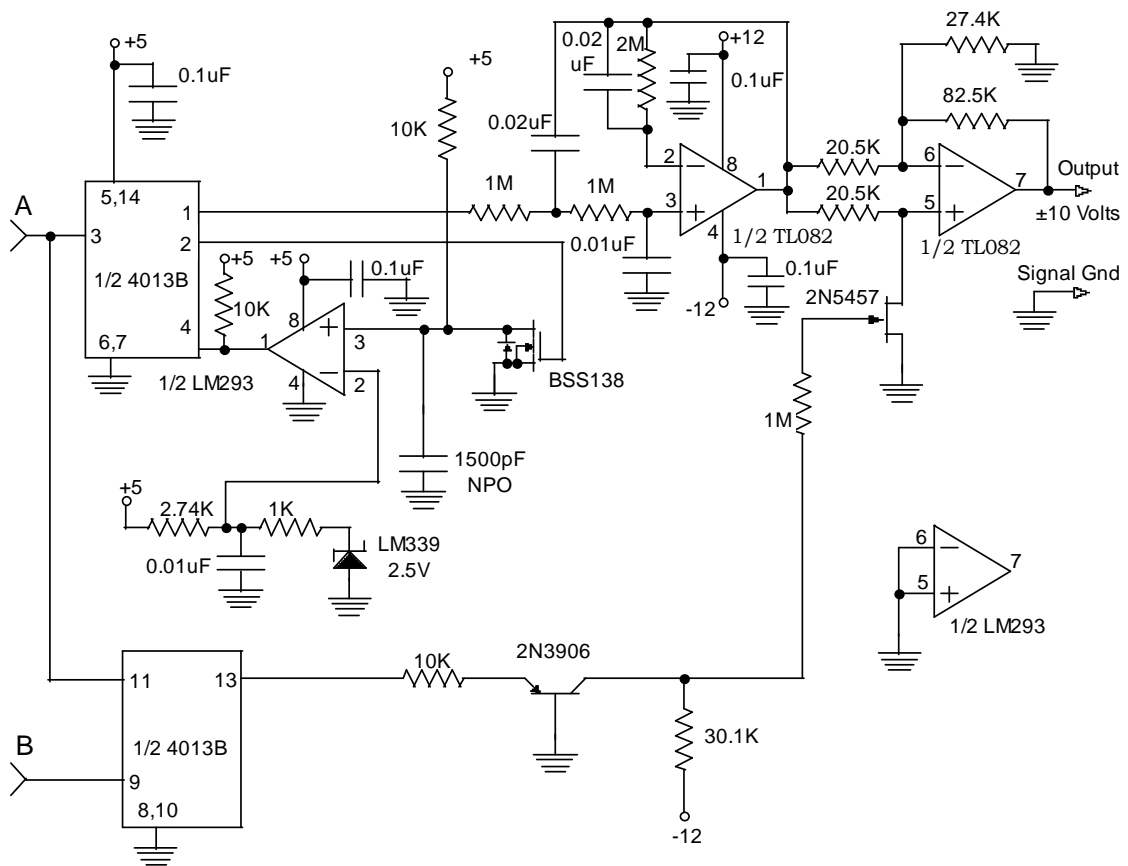
Do not use the new “A” output on the direction flip-flop. Use the original “A” and “B” signals from the encoder.



**The other improvement is designed to give the pulse generator a constant average voltage per pulse rate no matter the changes in power voltage.**

The original circuit produced a constant pulse width with an amplitude equal to the power voltage. This is OK if the power voltage is constant, but not if it is merely almost constant. The difference in average voltage per pulse rate for 5.0 volts versus 5.1 volts is 2%. Adding one part and changing two resistor values will bring it down to 0.05%.

The circuit below allows some voltage change to the pulse reset voltage level (pin 2 of the LM293) to allow the pulse width to be reduced at the same rate as the power voltage increases. The values selected are centered on the supply being between 4.9 and 5.1 volts. Other resistor ratios may be used to center at other voltages.



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**Watson Industries, Inc.**  
**3035 Melby Street, Eau Claire, Wisconsin 54703 USA**  
**[www.watson-gyro.com](http://www.watson-gyro.com)**